## REMARKS

In the final Office Action, the Examiner rejected claims 1, 4, 9, 15-22, and 28 under 35 U.S.C. § 102(b) as anticipated by Wang (U.S. Patent No. 5,563,891); rejected claims 2, 3, 10, and 23 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Co et al. (U.S. Patent No. 5,602,882); and rejected claims 11-14 and 24-27 under 35 U.S.C. § 103(a) as unpatentable over Wang in view of Mays et al. (U.S. Patent No. 5,384,770). The Examiner allowed claims 37-45 and objected to claims 5-8 and 29-36 as dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include the features of the base claim and any intervening claims.

By this Amendment, Applicants propose amending claims 1, 2, 15, 16, and 28 to improve form. Applicants appreciate the Examiner's identification of allowable subject matter, but respectfully traverse the Examiner's rejections under 35 U.S.C. §§ 102 and 103 with regard to the claims as amended herein. Claims 1-45 remain pending.

In paragraph 2 of the Office Action, the Examiner rejected claims 1, 4, 9, 15-22, and 28 under 35 U.S.C. § 102(b) as allegedly anticipated by Wang. Applicants respectfully traverse the rejection.

Amended claim 1, for example, recites a combination of features of a system for reliably receiving data. The system comprises a memory, write logic, and read logic. The write logic is configured to receive data and an unreliable clock signal and write the data to the memory using the unreliable clock signal. The read logic is configured to generate a data enable signal and a gapped clock signal that is generated by turning on and off a constant local clock signal, where the gapped clock signal is used to recover the data. The read logic comprises a read register to

receive the data enable signal and the constant local clock signal and read the data from the memory based on the data enable signal and the constant local clock signal.

A proper rejection under 35 U.S.C. § 102 requires that a single reference teach every aspect of the claimed invention either expressly or impliedly. Any feature not directly taught must be inherently present. In other words, the identical invention must be shown in as complete detail as contained in the claim. See M.P.E.P. § 2131. Wang does not disclose or suggest the combination of features recited in amended claim 1. For example, Wang does not disclose or suggest read logic that comprises a read register to receive a data enable signal and a constant local clock signal and read the data from the memory based on the data enable signal and the constant local clock signal. Instead, Wang discloses reading data from memory using a gapped read clock (Fig. 3; col. 2, lines 47-60).

For at least these reasons, Applicants submit that claim 1 is not anticipated by Wang. Claims 4 and 9 depend from claim 1 and are, therefore, not anticipated by Wang for at least the reasons given with regard to claim 1.

Amended independent claim 15 recites a combination of features of a system for reliably receiving data. The system includes means for receiving data and an unreliable clock signal, means for writing the data to a memory using the unreliable clock signal, means for generating a reliable clock signal by turning on and off a local clock signal, means for generating a data enable signal, means for reading the data from the memory using the data enable signal and the local clock signal, and means for recovering the data based on the reliable clock signal.

Wang does not disclose or suggest the combination of features recited in amended claim 15. For example, Wang does not disclose or suggest means for recovering the data based on the

reliable clock signal. Instead, Wang discloses demultiplexing a higher rate signal to obtain lower rate signals (col. 4, lines 37-41). Wang does not disclose or suggest that this demultiplexing to obtain lower rate signals is based on a reliable clock signal generated by turning on and off a local clock signal, as required by claim 15.

For at least these reasons, Applicants submit that claim 15 is not anticipated by Wang.

Amended independent claim 16 recites a combination of features of a method for recovering data. The method comprises receiving data and an unreliable clock signal, writing the data to a memory using the unreliable clock signal, providing a first state machine to generate a gapped clock signal by turning on and off a constant local clock signal, providing a second state machine to generate a data enable signal, and reading the data from the memory using the data enable signal and the constant local clock signal.

Wang does not disclose or suggest the combination of features recited in amended claim 16. For example, Wang does not disclose or suggest providing a first state machine to generate a gapped clock signal by turning on and off a constant local clock signal or providing a second state machine to generate a data enable signal. In fact, Wang is completely silent with regard to a state machine.

For at least these reasons, Applicants submit that claim 16 is not anticipated by Wang. Claims 17-22 depend from claim 16 and are, therefore, not anticipated by Wang for at least the reasons given with regard to claim 16.

Amended independent claim 28 recites a combination of features of a receiver. The receiver comprises a reliable clock generator and a receiver component. The reliable clock generator is configured to receive data and an unreliable clock signal, write the data to a memory

using the unreliable clock signal, generate a reliable clock signal from a constant clock signal, generate a first enable signal, read the data from the memory using the first enable signal and the constant clock signal, and output the data and the reliable clock signal. The receiver component is configured to receive the data and the reliable clock signal from the reliable clock generator and recover the data based on the reliable clock signal.

Wang does not disclose or suggest the combination of features recited in amended claim 28. For example, Wang does not disclose or suggest a receiver component that is configured to receive the data and the reliable clock signal from the reliable clock generator and recover the data based on the reliable clock signal. The Examiner alleged that data pump 650 in Figure 3 of Wang is equivalent to the receiver component (final Office Action, page 5). Applicants disagree.

At column 4, lines 23-36, Wang discloses:

> In any event, the average rate of the gapped read clock over a long period of time is approximately the same as the data rate of the incoming data of the lower rate signal. Therefore, the likelihood of slips is dramatically reduced or eliminated. The data read out of the elastic buffer 620 in synchronism with the gapped read clock is multiplexed with other like signals by the data pump 650 to produce a higher rate signal. As discussed above, each channel of the higher rate signal has extra stuffing bits for storing a null bit or a data bit. The data bits read out in synchronism with the gapped read clock are placed in the payload bit positions and the stuffing bit positions of the corresponding channel. The higher rate signal is then transmitted to the desynchronizer 70.

Wang does not disclose or suggest that data pump 650 is configured to receive data and a reliable clock signal from a reliable clock generator and recover the data based on the reliable clock signal, as required by claim 28. Instead, Wang discloses that data pump 650 multiplexes data with other lower rate signals to generate a higher rate signal (col. 4, lines 27-30).

For at least these reasons, Applicants submit that claim 28 is not anticipated by Wang.

In paragraph 3 of the final Office Action, the Examiner rejected claims 2, 3, 10, and 23 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Co et al. Applicants respectfully traverse the rejection.

Claims 2, 3, 10, and 23 variously depend from claims 1 and 16. The disclosure of Co et al. does not cure the deficiencies in the disclosure of Wang as noted above with regard to claims 1 and 16. Claims 2, 3, 10, and 23 are, therefore, patentable over Wang and Co et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1 and 16. Claims 2, 3, 10, and 23 are further patentable for reasons of their own.

For example, claim 3 recites that the memory includes a first-in, first-out memory. With regard to claim 3, the Examiner alleged that Co et al. discloses a first-in, first-out memory (final Office Action, page 7). Applicants submit that the Examiner has not established a prima facie case of obviousness.

To establish a prima facie case of obviousness under 35 U.S.C. § 103 based on a combination of references, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of the references (M.P.E.P. § 2143). According to M.P.E.P. § 2143, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. In this case, the Examiner provided absolutely no motivation for adding the alleged first-in, first-out memory of Co et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

Claim 10 recites, among other things, that the read logic is configured to generate an error signal when overflow conditions occur in the memory. With regard to claim 10, the Examiner alleged that Co et al. discloses generating a data error when overflow conditions occur (final Office Action, page 7). Again, the Examiner provided absolutely no motivation for adding the alleged "generating a data error when overflow conditions occur" of Co et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

Similar deficiencies exist in the Examiner's rejection of claim 23. In other words, the Examiner provided no motivation for combining the alleged features of Co et al. and Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

In paragraph 4 of the Office Action, the Examiner rejected claims 11-14 and 24-27 under 35 U.S.C. § 103(a) as allegedly unpatentable over Wang in view of Mays et al. Applicants respectfully traverse the rejection.

Claims 11-14 and 24-27 depend from claims 1 and 16, respectively. The disclosure of Mays et al. does not cure the deficiencies in the disclosure of Wang as noted above with regard to claims 1 and 16. Claims 11-14 and 24-27 are, therefore, patentable over Wang and Mays et al., whether taken alone or in any reasonable combination, for at least the reasons given with regard to claims 1 and 16. Claims 11-14 and 24-27 are further patentable for reasons of their own.

For example, claim 12 recites that the read logic is further configured to determine that the write logic has received the unreliable clock signal before the counter reaches a predetermined count and turn on the constant local clock signal. With regard to claim 12, the Examiner alleged that Mays et al. discloses determining that write logic has received data before a counter reaches a predetermined count (final Office Action, page 8). Again, the Examiner

provided absolutely no motivation for adding the alleged "determining that write logic has received data before a counter reaches a predetermined count" of Mays et al. to the system of Wang. For at least these reasons, the Examiner's rejection is improper and should be withdrawn.

Claims 13 and 14 recite that the read logic is further configured to determine that the counter has reached a predetermined count and turn on the constant local clock signal and disable the data enable signal and that the read logic is further configured to wait for the write logic to receive the unreliable clock signal before enabling the data enable signal and reading data from the memory, respectively. With regard to claims 13 and 14, the Examiner alleged that Mays et al. discloses determining that the counter has reached a predetermined count (final Office Action, page 8). Again, the Examiner provided absolutely no motivation for adding the alleged "determining that the counter has reached a predetermined count" of Mays et al. to the system of Wang. For at least these reasons, the Examiner's rejections are improper and should be withdrawn.

Similar deficiencies exist in the Examiner's rejections of claims 24-27. In other words, the Examiner provided no motivation for combining the various alleged features of Mays et al. and Wang. For at least these reasons, the Examiner's rejections are improper and should be withdrawn.

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and allowance of pending claims 1-45.

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 1-45 in condition for allowance. Applicants submit that the

entry of this Amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

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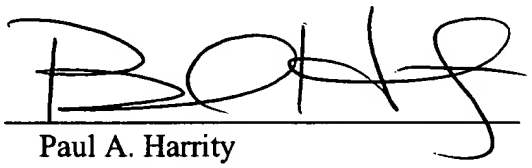
By: 
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